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Fabrication and Testing of ISFET Based pH Sensor for Microliter Scale Solution Targets

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***Abstract*—In recent years, there has been an increasing interest in the monitoring and controlling of pH. It has become an important aspect of many industrial wastewater and water quality treatment processes. At the same time, the demand for smaller electronic devices used for various industrial, commercial, and research applications has greatly increased. In this paper, we propose a fabrication method of Ion-Sensitive Field Effect Transistor (ISFET) using MEMS techniques for pH sensing application. The novelty of this device lies in the detection of target solution with volumes in the sub-micro liter range. This achievement has the potential to satisfy the research demands in various areas including chemistry, biology and medicine. Nanomaterials, such as Carbon Nanotubes (CNTs) with excellent electrical, mechanical, and thermal properties can be incorporated to these small ISFET devices through certain nano techniques including Atomic Force Microscopy (AFM) based surface nanomachining and Dielectrophoresis (DEP). With proper electrical packaging, our ISFET chip has been able to detect the pH values of 2.5 μl solutions. The results reveal a linearity of pH measurement with a corresponding sensitivity of 10.7 mV/pH.**

I. Introduction

SINCE Bergveld introduced the Ion-Sensitive Field Effect Transistor (ISFET) in 1970 [1], the sensor industry has expanded rapidly. The concept upon which the ISFET works has a variety of applications, including those in the medical field, food industry, wastewater treatment processes, and soil nutrient analysis [2]. The durability, quick response time, accuracy, and small size of ISFETs make them more advantageous to use than conventional glass electrode pH sensors. Additionally, they are less expensive to manufacture [3]. Because of the widespread use of ISFETs, much attention has been given toward making them smaller, more sensitive, and more efficient. Reducing their size would open new possibilities for incorporating them into smaller electronics such as personal drug monitoring devices [3]. At the same time, smaller devices would allow for the analysis of smaller targets, thereby reducing unnecessary waste of the sample solution.

ISFET based pH sensor is one of the most well-known applications [4-5]. The concept of the ISFET is easily understood by comparing it to a Metal-oxide Semiconductor Field-Effect Transistor (MOSFET) [6]. Although these two devices have the same equivalent circuit, there are still some key differences in their designs. As shown in Fig.1, a reference electrode and an ion-sensitive membrane in the ISFET take the place of the metal gate in a MOSFET. When a solution contacts the ISFET gate insulator membrane, an ion interaction occurs that results in a voltage being applied to the gate. This ion activity at the solution-membrane interface is described by the Nernst equation. Under the gate voltage, a conducting channel forms between the source and drain, allowing current to flow through the device. As the ion activity at the membrane changes, the gate voltage changes also, and the drain current is a unique function of the gate voltage. Therefore by measuring the change of the gate voltage while adjusting the gate voltage to keep the drain current constant, the ion concentration of the solution can be determined [7].

Furthermore, with more and more study on CNTs, we believe CNTs with high current carrying capacity may have a huge potential to produce more compact and powerful devices for pH measurement applications based on ISEFT. However, CNT based ISFET for pH control application has not yet been explored. If this is made possible, it will be a significant contribution for applications in various areas, including medicine, biology, chemistry, medicine and industry.

The objective of this paper is to fabricate ISFET structure in 1.2 mm × 0.7 mm area and obtain the pH measurement sensitivity. The gate area, which is the gap of 40 μm between the source and drain, can be used to contact with target solution in micron liter scale. The inversion layer share the same length of 40 μm, which ensures the feasibility that nanochannels can be fabricated to connect the source and drain as AFM is able to carry out surface nanomachining easily within that size. In the future, a bundle of CNTs will be aligned in the nanochannel by the means of DEP in order to seek an improved performance.

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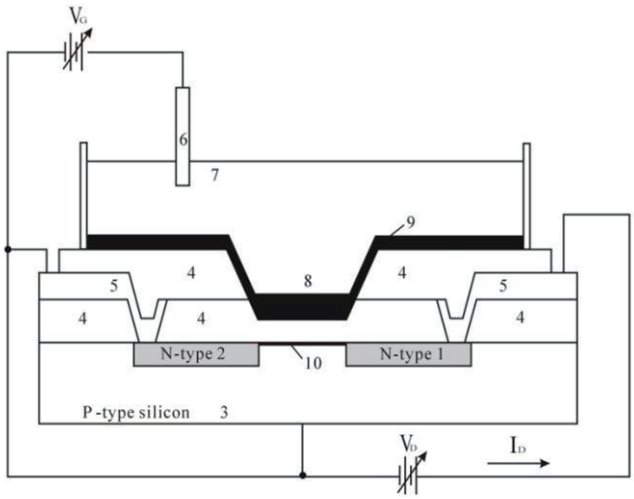

Fig.1. Schematic diagram of a composite gate, dual dielectric ISFET: 1 drain; 2 source; 3 substrate; 4 insulator; 5 metal contacts; 6 reference electrode; 7 solution; 8 electroactive membrane; 9 encapsulant; 10 inversion layer.

II. Fabrication of ISFET

The fabrication process of our ISFET consists of eight major steps, all of which were completed using the cleanroom thin film facilities in High Density Electronics Center (HiDEC) of University of Arkansas. The fabrication started with a 5-inch p-type boron diffused silicon wafer with orientation of <1-1-1> and thickness of 625 µm. The eight major steps are Field Oxidation, Phosphorus Source Preparation, Pre-Deposition of Diffusion Drive-in, Gate Oxide, Backside Oxide Etch, Lift-off PR Patterning, and Metallization as shown in Fig. 2. The multilayer mask was designed using AutoCAD and were produced in both clear field and dark field polarities.

A. Field Oxidation

During the fabrication, a diffusion furnace (Bruce BDF4, Bruce Technologies Inc., USA) was used for oxidation and phosphorus diffusion. In filed oxidation, multi bare silicon wafers were loaded into the furnace for oxidizing, one of which would be used as the process wafer. The objective of field oxidation is to grow a silicon dioxide layer of about 500 nm thick on wafer's polished side. After loading the wafers and heating inside the oxidation tube of the furnace at 750 °C for 50 minutes, the process wafer underwent a DCE clean, which helps the wafer trap or remove metal substances or other impurities. Then, the temperature was increased to 1100 °C to complete dry oxidation and wet oxidation for 40 minutes and 34 minutes, respectively. Finally, the tube was cooled to 750 °C for 55 minutes, and the wafer was unloaded. Through Nanospec microscopy, the thickness of oxidation layer was about 5430 Å on the polished side. The oxidation on both sides of the process wafer would work as a protection layer during the next diffusion process.

B. Phosphorus Source Preparation

The phosphorus source preparation was done in a specific

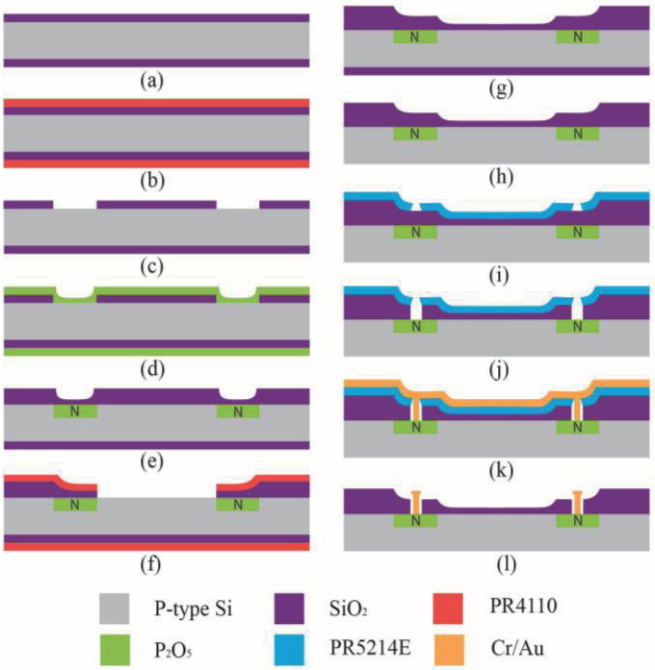

Fig. 2. Diagram of the fabrication of ISFET: (a) oxidation, (b) apply PR, (c) pattern for diffusion, (d) pre-deposition of dopant, (e) dopant drive-in, (f) pattern for gate, (g) gate oxidation, (h) backside oxide etch, (i) lift-off PR pattern, (j) oxide etch on doped area, (k) metal deposition, and (l) lift-off.

- phosphorus tube that was different from the oxidation one. The source wafer was a PH-950 n-type 5-inch wafer with active component of SiP_2O_7. The source wafer was loaded into the tube on a boat with 2 dummy wafers located on its edges. The tube was first dried in N_2 at 400 °C for 1 hour. Then, the temperature rose to 885 °C in 50 minutes, and it was followed by maintaining the temperature at 885 °C for 18 hours with both N_2 and O_2 valves on. Then, the tube temperature was decreased to 400 °C for 1 hour before loading the process wafer. After this process, the tube was filled with the dopant vapor P_2O_5 from the source by direct volatilization.

C. Pre-Deposition

It is necessary to open windows for diffusing the silicon wafer by etching the oxidation layer using photolithography before the wafer goes through the pre-deposition process. The wafer was first coated by AZ 4110 positive Photoresist (PR) by a desktop spin coater at maximum rpm of 3000 for 30 seconds. Before coating, a hexamethyldisilazane (HMDS) process for was implemented for the silicon wafers in order to provide an adhesion promoter for PR. The coating process gave a 1.25 µm hick PR layer. Then, the coated wafer was baked and transferred to the aligner (SUSS MA 150). The first mask (NDIFF, darkfield) was used to pattern the PR by exposing for 6 seconds, and the exposed PR was developed. In order prevent the silicon dioxide layer on the backside from being etched during etching the frontside, it was coated by a layer of PR and baked inside a Blue M Oven at 110 °C for 20 minutes. Next, the open areas on the front side were ready to be etched by Buffered Oxide Etch (BOE) 5:1, the etching rate of which is 1000 Å/min. After the wet etching,

the entire PR was stripped off by immersing the wafer into a positive resist stripper (Baker PRS-1000) solution at 85 °C for 10 minutes. Eventually, the wafer was loaded to the phosphorus tube. The deposition begun at 700 °C for 30 minutes, and then the temperature was increased to 885 °C for 65 minutes. The deposition ended with another 35 minutes treatment at 700 °C. Thus, the wafer was uniformly covered by the dopant. During the entire furnace process, N_2 was the only gas needed.

Besides the process wafer, a control wafer C1, which was a bare silicon wafer of the same kind as the process wafer, was also loaded in this process in order to investigate the diffusion quality. After unloading both wafers, they underwent a deglaze process by immersing them into a mixture solution of 1000 mL DI water and 100 mL HF at room temperature for 2 minutes. The deglaze was used to remove the excess un-reacted dopant.

D. Diffusion Drive-in

The dopant deposited on Si diffused in this step by loading the control wafer and the process wafer into the phosphorus tube at high temperatures with N_2 and O_2 gas flow. The wafers were first heated at 1000 °C for 30 minutes with N_2 and another 30 minutes with O_2. After the dry oxidation, a wet oxidation with steam flow was done for 20 minutes at the same temperature. Finally, the temperature was decreased to 750 °C for 35 minutes with N_2. After the drive-in, the wafers were covered by a thin SiO_2 layer. Thickness of SiO_2 on C1 and the process wafer were 924 Å and 4009 Å respectively after the completion of diffusion. The SiO_2 thickness on C1 is supposed to be the same as the one on the diffused areas on the process wafer.

Besides measuring the thickness of SiO_2, C1 was also used to calculate the junction depth, for which a groove is need on the doped silicon surface. The junction sectioning geometry is illustrated in Fig. 3. The oxidation layer on C1 was firstly removed by BOE 5:1 wet etching, and a groove was fabricated by using a wafer groover for 5 minutes. The blade of wafer groover has a radius of 19885 μm, and the groove depth was 16 μm measured by Dektak 3030 as shown in Fig. 4. The solution of $CuSO_4$*$5H_2O$ with HF was prepared as the n-type stain. A stain droplet was applied to the groove area, and C1 was taken to the aligned to be exposed for 390 seconds. Then, the stain was removed by dipping into DI water and blow-dry with N_2. The copper plating on the doped area was inspected by microscopy. As shown in Fig. 5, the copper plating was obvious to present the outline of the groove after the stain was exposed and rinsed off. Next, a microscope with micro-measure function was employed to determine W_1 and W_2, which were 1692.4 μm and 1442.7 μm respectively. According to the geometry in Fig. 3, the junction depth x_j was able to be calculated using equation (1). Ultimately, the junction depth on C1 was obtained, x_j = 4.9 μm.

$$x_j = d_2 - d_1 = \sqrt{r^2 - \left(\frac{W_2}{2}\right)^2} - \sqrt{r^2 - \left(\frac{W_1}{2}\right)^2} \qquad (1)$$

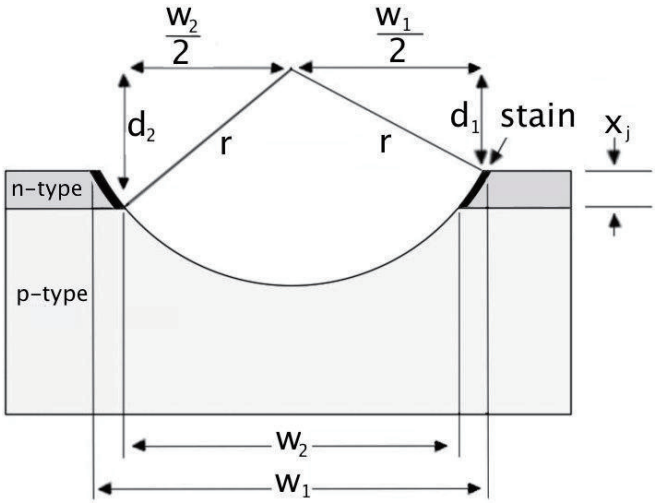

Fig. 3. Junction sectioning geometry.

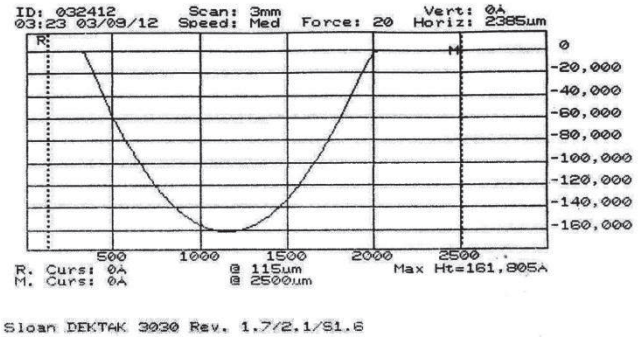

Fig. 4. Groove depth measurement by Dektak.

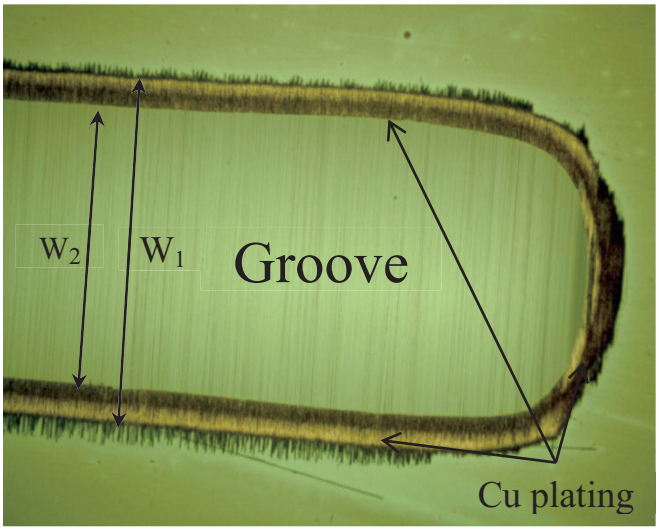

Fig. 5. Inspection (top-view) of Cu plating after junction stain applied on control wafer C1 by microscopy.

E. Gate Oxide

After the diffusion was complete, the thickness of oxidation layer on the process wafer was about 4009.4 Å

except for those doped areas, where the thickness was about 923.6 Å. Since the direct contact between target solutions and the transistor happens on the gate area, a fine thin oxide layer is needed instead of the current thick layer. Thus, the second mask (GATE, darkfield) was used to pattern the PR after coating and exposing 4110 on the frontside. HMDS and baking were done before and after coating respectively. After exposing the PR with the GATE mask for 6 seconds, the PR was developed for 45 seconds. Before etching, the backside was again coated by PR the same way as in Pre-Deposition. During etching, the process wafer was immersed into 1000 ml BOE 5:1 solution for 5 minutes to remove the uncovered SiO_2. Then, the PR was completely removed by PRS-1000, and the wafer was ready to go back to the furnace for oxidation with a second control wafer C2, another bare silicon wafer. Besides DCE clean, the gate oxidation process only involved dry oxidation with O_2 flow at 1100 °C for 40 minutes. Then, the temperature was decreased to 400 °C for 3 hours. Based on the oxidation thickness measurement through Nanospec microscopy, the gate area has about 560-Å-thick oxidation layer in the process wafer, while the thickness of oxidation layer on the diffused areas is about 1310 Å.

F. Backside Oxide Etch

In order to protect the oxidation layer on the front side during etching the oxidation off the backside of the process wafer, the frontside was coated with 4110 by spin coater after going through HMDS process. The coated wafer was baked at 110 °C for 2 minutes and immersed into 1000 ml BOE 5:1 solution for 7 minutes to remove the oxidation on the back completely. Then, a flood exposure and 3 minutes developing were used to strip off the entire PR.

G. Lift-off PR Patterning

In order to pattern the metal layer using lift-off, an image reversal photoresist AZ 5214E [8] was used. This special photoresist is intended for lift-off techniques, which call for a negative wall profile. Although AZ 5214E is still a positive photoresist comprised of a novolak resin and naphthoquinone diazide as Photo Active Compound (PAC), it is capable of Image Reversal (IR) resulting in a negative pattern of mask. Actually, AZ 5214E is almost exclusively used in the IR-mode. The IR-mode can be activated by baking and exposing the PR twice, and at the same the IR-mode can cause a lower dissolution rate at the top a higher rate at the bottom. Consequently, there will be a negative wall profile ideally suited for lift-off.

Before coating the process wafer with 5214E, the wafer was cleaned using acetone on a spin coater and underwent an HMDS process. Then, the PR was applied to the wafer using spin coater at 4000 rpm for 30 seconds, which gave a 2 µm thickness. Then, the coated wafer was baked at 88 °C for 45 seconds before apply the first exposure. The third mask (MET, Clearfield) was used to expose the PR for 6 seconds. It was followed by the IR baking, where the wafer was baked at 106 °C for 45 seconds. Next, the second exposure, a flood exposure with a blank glass wafer, was completed for 45 seconds to turn on IR-mode of 5214E. Then, the PR was developed using MF CD-26 developer for 45 seconds. Thus, the PR that was exposed only once was developed, and the wafer was ready for metallization.

H. Metallization

Metallization was realized using thermal evaporation (Edwards 306 Turbo). Chromium and gold were deposited onto the process wafer. The chromium as an adhesion layer was 15 nm thick, and the gold layer was about 233.8 nm thick. One of the major advantages of evaporation over other deposition methods, for example sputtering, is that the PR can survive during evaporation process and be used for lift-off. To lift off the metal, an ultrasonic cleaner was used. The process wafer was put into a crystallizing dish which was filled with acetone. Then the dish was moved into the ultrasonic cleaner and floated on the top of water. The ultrasonic was turned on for 5 minutes, and the metal started to be lifted off. The ultrasonic process could last longer until the metal is no longer lifted off, and the acetone in crystallizing dish should be replaced if necessary. Next, the wafer was rinsed with acetone and isopropyl alcohol (IPA). After the metallization step, our ISFET structure was completed as shown in Fig. 6. The thickness of metal layer was also measured using Dektak, and the gold layer was about 2000 Å above the silicon dioxide layer on the doped area as shown in Fig. 7.

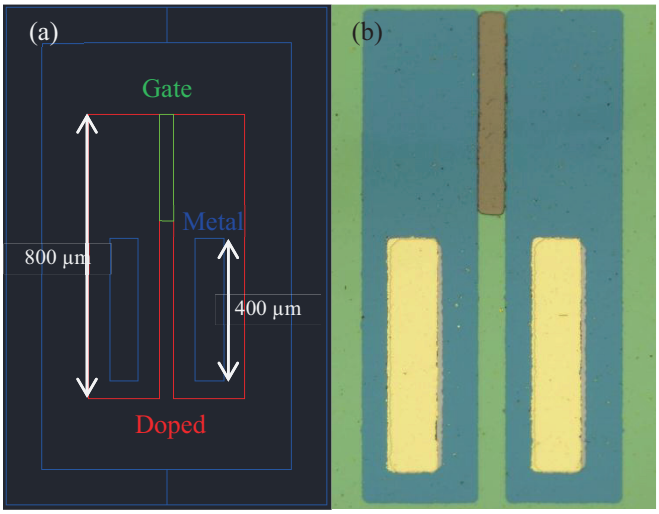

Fig. 6.Structure of ISFET: (a) desired and (b) fabricated.

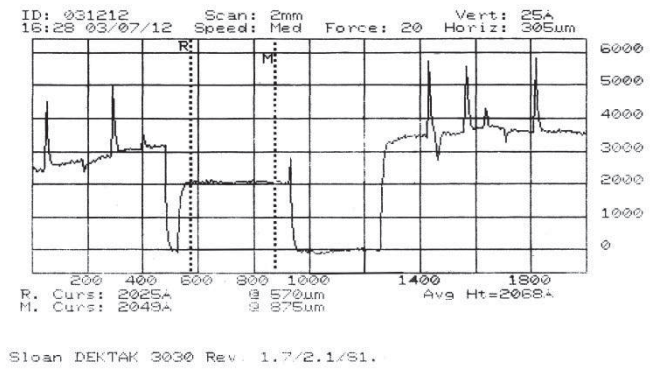

Fig. 7. Au thickness measurement above doped area using Dektak.

III. Experimental Setup

After cutting the process wafer into pieces of ISFET chip using a dicing saw, a small outline integrated circuit package (CSO00802, Spectrum Semiconductor Materials Inc., USA) was employed in order to establish reliable electrical connections, through which outer electronic devices could be applied. Fig. 8(a) shows the schematic of setup. There is a metal layer on top of the package cavity, and the cavity area fits more than two ISFET chips. Two ISFET chips were attached onto the cavity surface by conductive epoxy. Then, as shown in Fig. 8(b) the gold on the doped areas of the two chips and the metal layer on the package cavity were bonded to different pins through a wire bonder (Model 4123, Kulicke & Soffa, Singapore), which provides 25.4 µm diameter aluminum wire bonding. During the pH measurement, this structure employs a discrete null-balancing method and the output of ISFET, drain current I_d, will be held constant by adjusting the gate voltage V_{gs}. When gate area of the ISFET chip is exposed to various target solutions, the external bias voltage V_{gs} in series with the reference electrode should be adjusted to secure zero change of I_d. Therefore, the change of V_{gs} depends directly on the ionic activity/concentration. In this experiment, the drain voltage V_{ds} was constant at 1 V provided by a DC power supply (Model XP-760, Elenco Electronics Inc., USA), and I_d is measured by a picoammeter (Model 6485, Keithley, USA). A second DC power supply (Model N5748A, Agilent, USA) with a fine adjustable function at 0.01 V was employed to adjust V_{gs}. A copper wire in diameter of 250 µm (Model 93-2972, Strem Chemicals, USA) was used to detect target solutions. Thus, our ISFET is ready for measuring pH of any target solution.

IV. Current Results

Before testing, six target solutions were prepared. Their pH values were calibrated using a pH tester (pH55, Milwaukee Instruments, USA) and were 4.1, 5, 6, 7.1, 8.5, and 9.5 respectively. In order to test the ISFET, five droplets of 2.5 µL from each target solution were dropped onto the gate area and measured. For instance, a droplet from pH 4.1 solution was located onto the gate area using a pipette while the drain voltage was applied at 1 V. Then, the reference electrode was inserted into the droplet while the gate voltage was applied

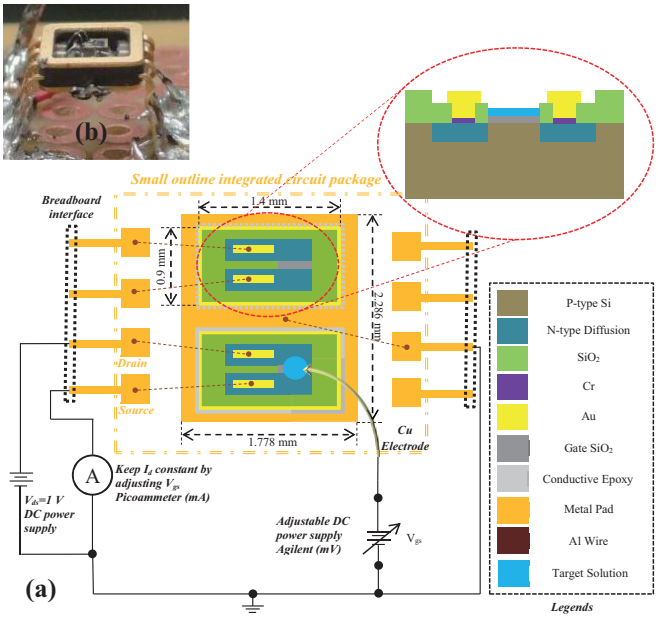

Fig. 8. Experimental setup for pH measurement: (a) schematic and (b) wire-bonded chip.

-and adjusted to keep the drain current constant at 5.475 mA. When the drain current was stabilized, the gate voltage was recorded. The droplet will evaporate quickly after the gate voltage is applied. Thus, the testing continued for the solution until five data were recorded. Then, the ISFET chip was stored overnight in a dry box (McDry MCU-201, Seika Machinery Inc., USA), where the relative humidity can be as low as 1 %. Then, the measurement for next pH solution could be carried out next day. Eventually, the complete results for pH detections between 4.1 and 9.5 were given in Table I. Furthermore, the corresponding Δ V_{gs} at each pH was collected to apply a linear fit in order to study the sensitivity of the ISFET as shown in Fig. 9. According to the linear fit, the slope is 0.0107, which means the sensitivity is 10.7 mV/pH. Additionally, the ISFET had an instant response. During the measurement, the reading varied immediately after the electrode was in contact with the target solution.

TABLE I
Results of pH Measurement Using ISFET

pH	V_{gs} (V)							
	#1	#2	#3	#4	#5	Mean	Stdev.	Δ V_{gs}
4.1	0.52	0.51	0.5	0.53	0.53	0.518	0.01304	-0.042
5	0.54	0.54	0.56	0.56	0.56	0.552	0.01095	-0.008
6	0.56	0.57	0.56	0.57	0.56	0.564	0.00548	0.004
7.1	0.56	0.56	0.55	0.57	0.56	0.56	0.00707	0
8.5	0.58	0.58	0.59	0.58	0.57	0.58	0.00707	0.02
9.5	0.6	0.59	0.58	0.58	0.58	0.586	0.00894	0.026

The entire measurement was completed under consistent conditions: Vds = 1 V and Id = 5.475 mA.

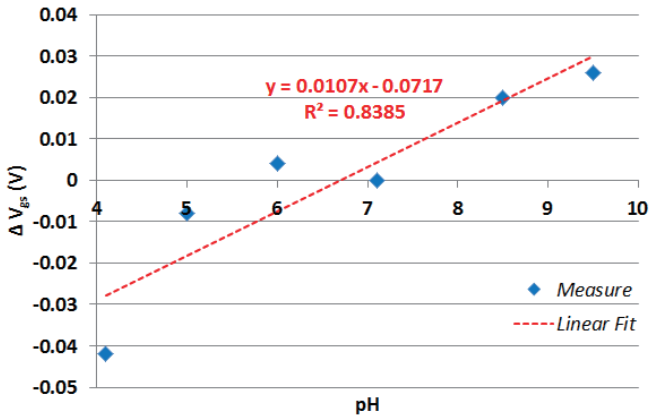

Fig. 9. pH response of a silicon dioxide gate ISFET.

V. Conclusion

ISFET chips have been successfully fabricated based on a 5-in-diameter p-type silicon wafer using MEMS fabrication techniques. N-type phosphorus dopants are diffused into the wafer to form the source and drain areas for each ISFET structure. The junction depth is measured, and the diffusion is verified. In addition, photolithography, evaporation, and lift-off techniques are involved during the fabrication. With a proper method of packaging, one of the ISFET chips has been tested as a pH sensor. The testing samples from six different solutions with pH values from 4.1 to 9.5 are as small as 2.5 µL. The experimental results indicate a linearity of pH measurement with a corresponding sensitivity of 10.7 mV/pH. Furthermore, our current ISFET provides us with a huge possibility that CNTs may be brought to the ISFET using AFM in order to improve the sensitivity.

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